HIGH FREQUENCY EVALUATION OF A RADIATION HARDENED CMOS 8-BIT FLASH ANALOG-TO-DIGITAL CONVERTER AT CRYOGENIC TEMPERATURES

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BACKGROUND

A radiation hardened CMOS 8-bit flash A/D converter is an attractive candidate device for future NASA deep space missions that require a significant level of radiation tolerance. This particular device has been considered by the Jet Propulsion Laboratory (JPL) for potential use on the MUSES CN (Mu Space Engineering Spacecraft) NASA/Japanese mission to Asteroid Nereus [1]. The purpose of this investigation was to determine the A/D converter suitability for use in a low temperature environment. The device was functionally tested over the temperature range (25 °C to –193 °C) in the Low Temperature Electronics facility at the NASA Glenn Research Center. Previous testing on the device was performed at a clock rate of 1 MHz [2]. Room temperature results showed that the A/D converter tracked the input voltage with an average offset of 34 mV [2]. This error is well within the overall error of the inaccuracies of the test setup. This error was the largest error measured for the A/D converter over the temperature range (23 °C to -193 °C). Overall test results at 1 MHz showed that the A/D converter operated properly down to –193 °C, well below the manufacturer's operating temperature of –55 °C [2].

The objective of this work was to repeat the low temperature testing on the radiation hardened CMOS 8-bit flash A/D converter at frequencies higher than 1 MHz. New test frequencies of 5, 10 and 20 MHz were selected. The maximum frequency identified by the manufacturer's data sheet was 20 MHz. During testing, noise problems were identified at the higher frequencies of 10 and 20 MHz; as a result, low temperature testing was limited to the 5 MHz clock rate. The experimental results are presented and discussed in this report.

TEST SETUP

Figure 1 shows the device layout and the corresponding test setup. This is the same setup used in the previous work [2]. Previous testing on the device was performed at a clock rate of 1 MHz [2]. The clock rate is set by a pattern generator. For each DC analog input value, the A/D converter produced an effective output bit pattern in binary format that was monitored by a logic analyzer. With a reference voltage (V_{REF}) of 4.0V, the A/D converter of Figure 1 has a 15.7 mV per bit measurement resolution. For simplification, only DC values from 0 to 4V (test vector) were applied to the analog input of the converter. Testing of the A/D converter was performed in a chamber whose temperature was controlled using liquid nitrogen as the coolant.

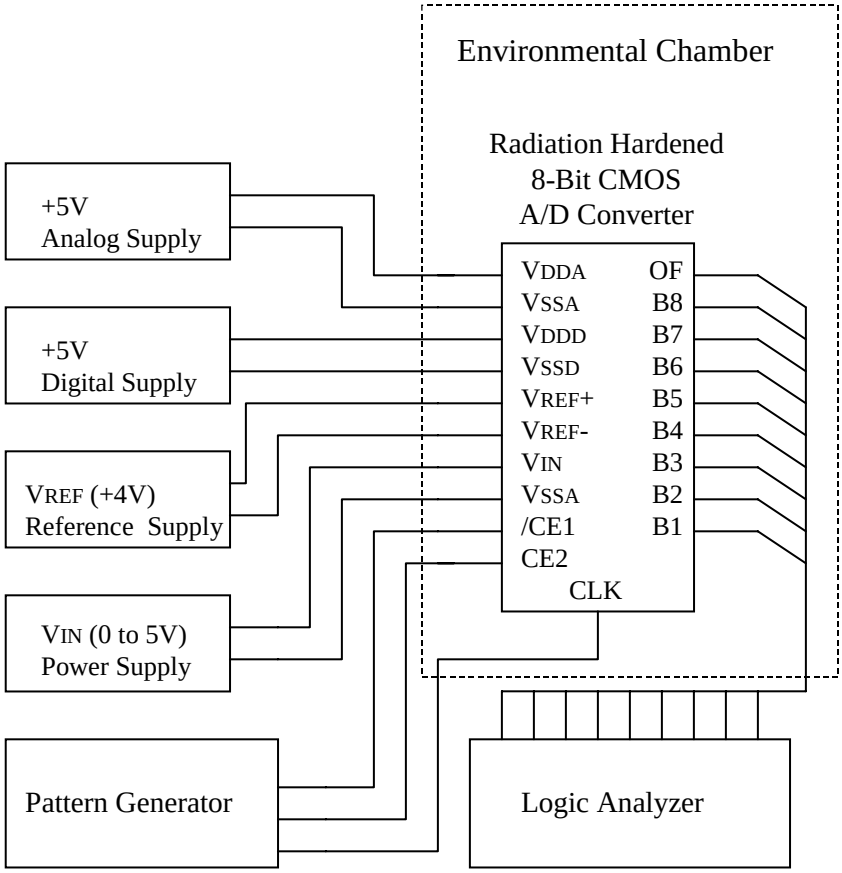

Figure 1. Test Setup for the radiation hardened 8-bit CMOS A/D converter.

RESULTS AND DISCUSSION

The pattern generator, which produces the input signals to the A/D converter, utilizes a 3 foot ribbon cable terminated into a TTL signal generator pod as shown in Figure 2. This Pod is then connected to a 18" twisted-pair flat ribbon cable, which is inserted into the environmental chamber and connected to the A/D converter test circuit board. A similar arrangement is made for A/D converter output signals to the logic analyzer.

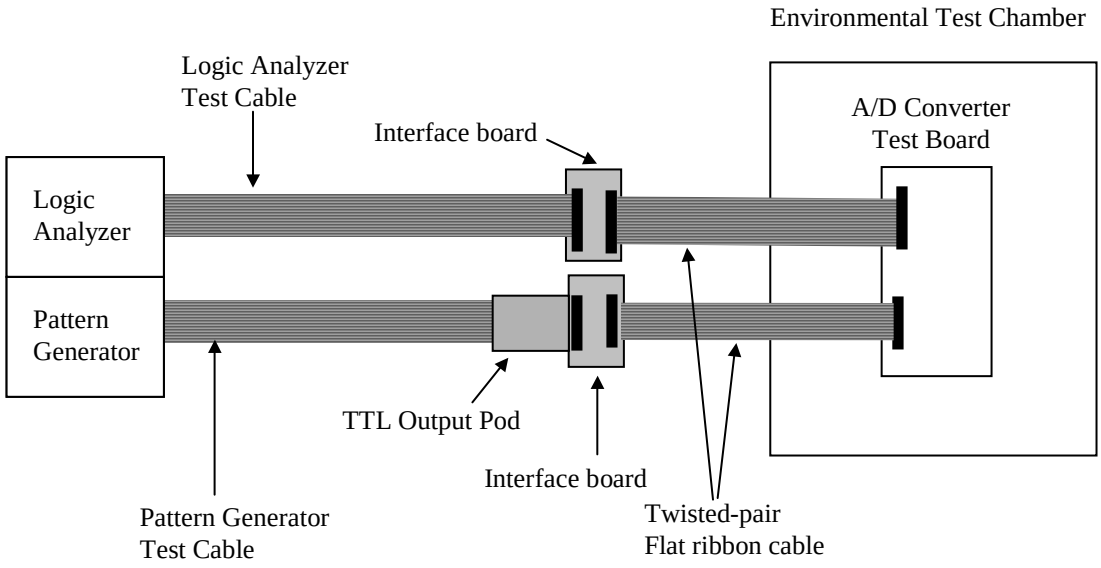

Figure 2. Input/Output Cabling.

This particular configuration results in a distorted clock signal at high frequency. Figure 3 shows the clock signal at different frequencies (1, 5, 10 and 20 MHz) for this particular setup. At 1 MHz the clock signal is fairly clean. At 5 MHz some level of signal distortion has occurred, but the signal is still usable for testing the A/D converter at the 5MHz clock rate. However, by 10 MHz, the clock signal displays a significant amount of distortion, and at 20 MHz, the clock signal is completely distorted. As a result, no testing was performed on the A/D converter at 10 and 20 MHz clock rates. This distortion of the clock signal can be attributed to long cable lengths involved in the setup. With proper line impedance terminations significant improvement in signal integrity is possible. In fact, the manufacturer of the pattern generator recommends line terminations. At the lower frequencies (i.e. 1MHz and below) line terminations were not needed for good signal integrity, as a result, no effort was put into providing line terminations. Designing proper line terminators for use within the environmental chamber may be difficult do to its extreme temperatures range. Line terminators may have to be placed just outside of the environmental chamber. An investigation into this problem, most likely, will be required for future high frequency test circuits.

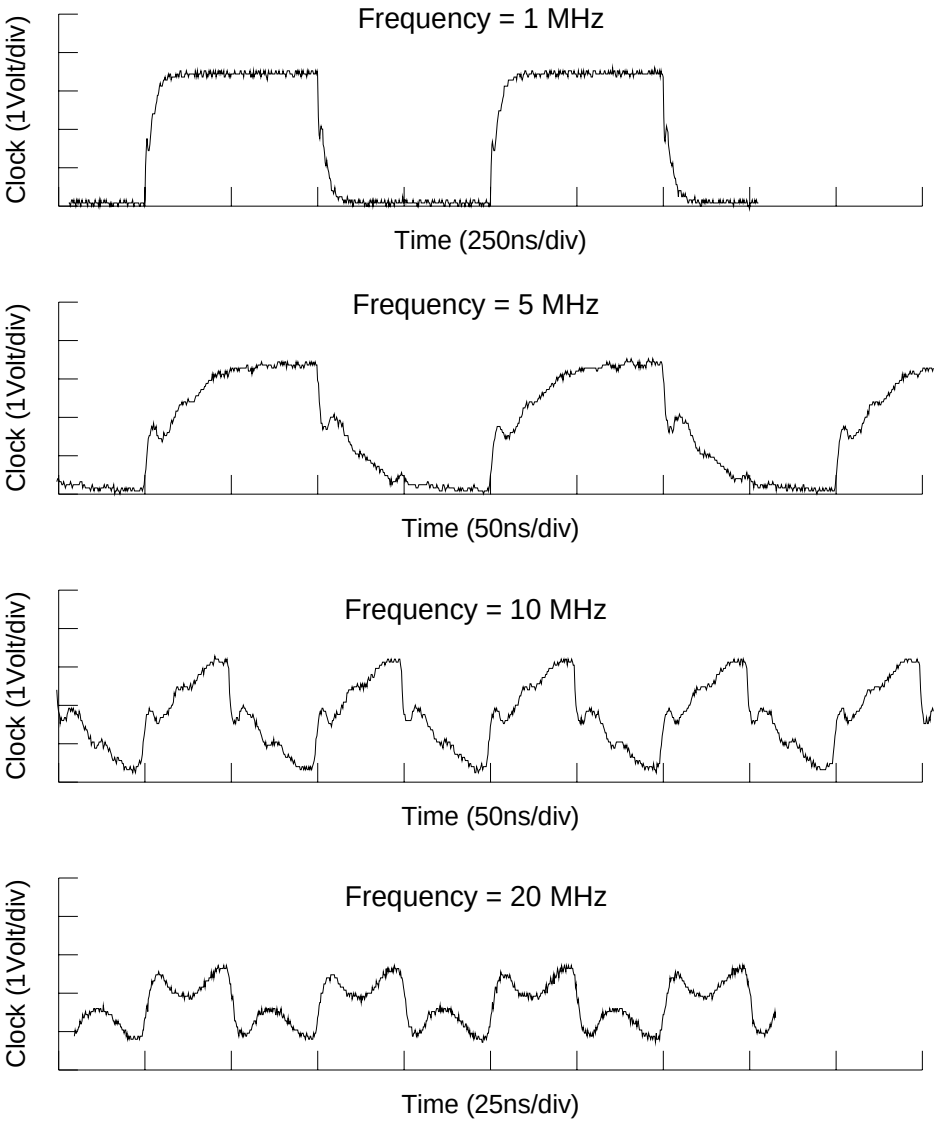

Figure 3. Different clock signals for A/D converter test setup.

Low temperature testing was performed on the radiation hardened 8-bit flash A/D converter at a clock rate of 5 MHz. Tables 1 through 3 show the voltage conversion capability of the A/D converter at 25C, -100C and –190C, respectively. Each table shows the applied input voltage (Vin), the binary value of the outputs, the calculated decimal output voltage (binary output $\times$ 15.7 mV/bit), and the difference or offset between the decimal output voltage and the input voltage at the specified temperature. In general, the A/D converter tracked the input voltage with an average offset of about 24 mV [2]. This error is well within the overall error of the inaccuracies of the test setup and very similar to results obtained at 1 MHz [2]. Some small jitter was noted in the logic analyzer readings for all temperatures, but was more noticeable at the –190 °C as seen in Table 3. This jitter most likely resulted from the small level of signal distortion in the clock and long cable lengths of the pattern generator/logic analyzer.

Table 1. Temperature = 25 °C Frequency = 5 MHz

Vin	binary Vout	decimal Vout (V)	Δ Vout -Vin (offset) (V)
0	1	0.016	0.016
1.00	65	1.02	0.02
2.00	129	2.02	0.02
2.50	161	2.53	0.03
2.75	177	2.78	0.03
3.00	193	3.03	0.03
3.98	255	4.00	0.02
		average offset =	0.024

Table 2. Temperature = -100 °C Frequency = 5 MHz

Vin	binary Vout	decimal Vout (V)	Δ Vout -Vin (offset) (V)
0	0	0.00	0.00
1.00	65	1.02	0.02
2.00	129	2.02	0.02
2.50	161	2.53	0.03
2.75	177	2.78	0.03
3.00	193	3.03	0.03
3.99	255	4.00	0.01
		average offset =	0.02

Table 3. Temperature = -190 °C Frequency = 5 MHz

Vin	binary Vout	decimal Vout (V)	Δ Vout -Vin (offset) (V)
0	0	0.00	0.00
1.00	62-65*	0.97 to 1.02	-0.03 to 0.02
2.00	127-130*	1.99 to 2.04	-0.01 to 0.04
2.50	159-161*	2.49 to 2.53	-0.01 to 0.03
2.75	175-177*	2.75 to 2.78	0.0 to 0.03
3.00	191-193*	3.00 to 3.03	0.00 to 0.03
3.98	254-255*	3.98 to 4.00	0.00 to 0.02
		average offset =	-0.006 to 0.024

* range of logic analyzer readings.

CONCLUSION

Testing was performed on the radiation hardened 8-bit flash A/D converter at a clock rate of 5 MHz over at temperature range of 25 °C to -190 °C. In general, the A/D converter tracked the input voltage with an average offset of about 24 mV [2] over the entire temperature range. This error is well within the overall error of the inaccuracies of the test setup and very similar to results obtained at 1 MHz [2]. Some small jitter was noted in the readings for all temperatures, but was more noticeable at the –190 °C. This jitter most likely resulted from the long cable lengths of the pattern generator/logic analyzer. For test frequencies above 5 MHz, line terminations will be required to maintain signal integrity. In conclusion, test results show that the A/D converter operates down to -190 °C at a frequency of 5 MHz, well below the manufacturer's operating temperature of –55 °C.

REFERENCES

[1] Discussions with JPL/NASA mission and project groups.

[2]. S. Gerber, A. Hammoud, R. Patterson, E. Overton, M. Elbuluk, R. Ghaffarian,R. Ramesham, and S. Agarwal, "Low Temperature Testing of a Radiation Hardened CMOS 8-Bit Flash Analog-To-Digital (A/D) Converter," 36rd IECEC, Savannah, Georgia, July 29–Aug 2, 2001.